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*sub
or*

31. (Amended) A device according to claim 28, wherein said first insulator film is thinner than said second insulator film, said first transistor is included in a logic circuit, and said second transistor is included in a memory cell.

*B
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cancel.*

32. (Amended) A device according to claim 28, wherein said first and second gate electrodes are connected to each other through a connection layer and top surfaces of said first and second gate electrodes and said connection layer are coplanar.

REMARKS

In the pending Office Action, claims 12 and 26-28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kume et al. U.S. Patent No. 5,188,976. Claims 29-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kume. The Examiner objected to claims 12 and 26-32 under 35 U.S.C. § 112. Claims 12, 26, and 29 have been canceled. Claims 30-32 have been amended. Claims 27, 28, and 30-32 remain pending.

The Examiner states “[t]he preliminary amendment is silent as to claims 1-11 and 13-25.” As stated by the Examiner, claims 1-11 and 13-25 were canceled by an amendment included in the request for filing a divisional application filed October 17, 2000. As a result, it was neither necessary nor appropriate to again cancel those claims in the Preliminary Amendment. Applicants request the Examiner to enter the amendment canceling claims 1-11 and 13-25 upon receipt of this response.

The Examiner suggests the specification contain a cross-reference to the related applications. The request for filing a divisional application filed October 17, 2000 contains, on page 2, an amendment to insert before the first line of the specification: --This is a division of application Serial No 09/105,958 filed June 29, 1998, all of which is incorporated by reference--. In response to the Examiner's suggestion, however, that statement has been amended to reference the U.S. patent that issued from the parent application.

35 U.S.C. § 112 Objection

The Examiner objected to pending claims 27, 28, and 30-32 as containing the improper Markish format language "and/or". Claims 27, 28, and 30-32 do not recite the term "and/or". Therefore, Applicants request that the Examiner withdraw the objection to claims 27, 28, and 30-32.

35 U.S.C. § 102(b) Rejection

Pending claims 27 and 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kume. For anticipation, a reference must teach each and every limitation of the claimed invention. Kume fails to anticipate claims 27 and 28 because Kume does not teach every limitation.

and fig. 18

The Examiner refers to the embodiment described in Figure 4 as teaching the claimed limitation. Kume in this embodiment teaches a semiconductor device comprising a substrate on which several transistors are formed. The first type of transistors formed on the substrate are MOS transistors. The MOS transistor comprises a thin gate oxide film 27 and a gate electrode 28 (col. 7, lines 46-59). The second type of transistors formed on the substrate are non-volatile memory transistors. The non-volatile memory transistor comprises a interlayer insulating film, floating gate electrode

17, and control gate electrode 21. The interlayer insulating film is formed of thin silicon oxide films 18 and 20, and a silicon nitride film 19 (col. 8, lines 8-25). Kume differs from claim 27 in the characterization of the different components of the transistors. Claim 27 recites "said first and second insulator films are different in at least one of thickness, material, and material composition and said first and second gate electrodes are different in at least one of material and material composition." Kume fails to anticipate claim 27 because it does not teach the above limitations.

First, Kume does not teach the first and second insulating films are different in at least one of thickness, material, and material composition. Kume teaches the insulating film of the non-volatile memory transistor is formed of thin silicon oxide films 18 and 20, and a silicon nitride film 19 (col. 8, lines 14-19). Kume also teaches the insulating film of the MOS transistor is formed of oxide film 27 (col. 7, lines 53-54). Kume does not teach that the oxide film of the MOS transistor is different in material or material composition than that of the insulating layer, which is formed of a type of oxide film, of the non-volatile memory transistor. Also, Kume discloses the thickness of the insulating layer of the non-volatile memory transistor but does not disclose the thickness of the insulating layer of the MOS transistor as being different from the thickness of the insulating layer of the other transistor (col. 8, lines 30-39). Kume only describes the thickness of the MOS transistor insulating layer as "thin" (col. 7, lines 46-59).

Second, Kume does not teach the first and second gate electrodes are different in at least one of material and material composition. The Examiner asserts "Kume describes...first and second electrodes made of different thickness and materials". The Examiner refers to elements 29,30 and 31, 32 of Figure 4 for support. Elements 29,30

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and 31,32 are not describing gate electrodes but source and drain regions. Kume fails to disclose the gate electrodes as being different in material or composition. In fact, Kume discloses gate electrodes 28 of the MOS transistors being of the same material (col. 7, lines 56-59, col. 8, lines 1-3). Therefore, because Kume fails to teach every limitation of claim 27, Kume fails to anticipate claim 27. Claim 27 is, therefore, allowable.

Rejected claim 28 is also allowable over Kume at least due to its dependence from claim 27.

35 U.S.C. § 103(a) Rejection

Pending claims 30-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kume. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The Examiner fails to establish a *prima facie* case of obviousness because Kume does not teach or suggest all the claim limitations or provide motivation to combine teachings. As discussed above, Kume fails to teach the first and second insulating films are different in at least one of thickness, material, and material composition and the first and second gate electrodes are different in at least one of material and material composition. In addition, the Examiner has not provided additional references meeting the deficiencies of Kume. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness.

Further in the rejection of claim 30, the Examiner states "Damascene is a well-known process and Kume describes several methods of forming gate electrodes by well-known methods." Applicants respectfully traverse the Examiner's assertion that damascene patterns are well-known in the art when used in forming gate electrodes of different material or material composition. Applicants request the Examiner to provide a reference showing the use of a damascene process in forming gate electrodes of different material or material composition. Even if a damascene process is well-known in the art (which the Applicants do not concede), the Examiner has not provided any motivation to combine the damascene process with Kume. The Examiner asserts Kume describes forming gate electrodes by well-known methods, but the Examiner has not provided rationale as to why damascene process would be used as one of the well-known methods.

Also in the rejection of claim 32, the Examiner admits the connection layer is not coplanar. The Examiner states "it is an obvious design choice to make the connection layer also coplanar if additional layers or devices are to be made on top of the electrodes and the connection layer." The Examiner admits the limitation is not taught by Kume but has not provided an additional reference showing the missing limitation or motivation to combine the teaching with Kume.

Therefore, in view of the preceding remarks, Applicants assert the Examiner has failed to establish a *prima facie* case of obviousness and claims 30-32 are allowable.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

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Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Attached hereto is a marked-up version of the changes made to the claims by this Amendment. The attachment is captioned "Appendix to Amendment of July 12, 2001."

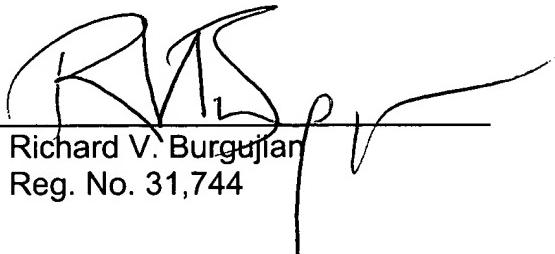
Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 12, 2001

By:

Richard V. Burgujian
Reg. No. 31,744

A handwritten signature in black ink, appearing to read "RVB", is written over a horizontal line. Below the line, the name "Richard V. Burgujian" and the registration number "Reg. No. 31,744" are printed in a smaller font.

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Appendix to Amendment of July 12, 2001

IN THE SPECIFICATION

On page 1, please amend the paragraph beginning before line 5 as follows:

This is a division of application Serial No 09/105,958 filed June 29, 1998, now U.S. Patent No. 6,184,083, [all of which are] which is incorporated herein by reference.

IN THE CLAIMS:

30. (Amended) A device according to claim [27] 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.

31. (Amended) A device according to claim [27] 28, wherein said first insulator film is thinner than said second insulator film, said first transistor is included in a logic circuit, and said second transistor is included in a memory cell.

32. (Amended) A device according to claim [27] 28, wherein said first and second gate electrodes are connected to each other through a connection layer and top surfaces of said first and second gate electrodes and said connection layer are coplanar.

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